Jointly Organized by
Electronics & ICT Academy

IIT Roorke, MNIT Jaipur, IIT Guwahati
http://www.mnit.ac.in/eict

Hybrid mode Programme
on
VLSI Design & Technology

May 11- May 22, 2025

Faculty Development Programme
Electronics & ICT Academy under aegis of

Ministry of Electronics and Information Technology
Government of India

meity.gov.in/content/schemes-projects

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Objective (Electronics & ICT Academy-Phase II)
1)To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.
2) To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.
3) To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India AI; National Programme on AI, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.
4) To promote standardization of FDPs through Joint Faculty Development Programmes.
5) To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.
6) To design, develop & deliver specialised FDPs on emerging technologies/ niche areas/ specialised modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multi-disciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of engineering and non-engineering colleges, polytechnics, ITIs, and PGT educators.

.ac.in/eict/)

An intensive 40 Hours Training Programme in online mode is being organized for faculty and doctoral students of engineering and technological institutions. It is also open to working professionals from industry/organizations. The main theme of training program will be oriented around exploring the state of the art methods for VLSI Design & Technology.

Experts/Speakers-

Speakers are from IITs, NITs, and IIITs, and industry experts from IBM.

Programme Modules:

Module 1 Foundation Modules: Before diving into chip design, programs ensure a strong grasp of the underlying physics and logic. Semiconductor Physics: PN junctions, MOS capacitor physics, and MOSFET characteristics (IV/CV curves). Digital Electronics: Combinational logic (mux, adders), sequential logic (flip-flops, FSMs), and timing analysis (setup/hold times). Computer Architecture: RISC vs. CISC, pipeline stages, and memory hierarchy (SRAM, DRAM, Flash).
Module 2: Front-End Design & Verification. This phase focuses on the "code" or logic that defines what the chip does. Hardware Description Languages (HDL): Extensive training in Verilog or SystemVerilog, RTL Coding: Writing synthesizable code for complex digital systems. Functional Verification: * Testbench development. UVM (Universal Verification Methodology): The industry standard for verifying complex designs. Assertion-Based Verification (SVA).
Module 3 Back-End (Physical Design): This phase focuses on how the design is physically laid out on a silicon wafer. CMOS Fabrication: Photolithography, etching, diffusion, and ion implantation. Physical Design Flow: * Floorplanning: Defining the chip boundary and pin placement. Placement & Routing (PnR): Mapping logic gates to physical locations and connecting them. Static Timing Analysis (STA): Ensuring the signals reach their destination within the clock cycle, Checks (DRC) to ensure the layout can be manufactured and Layout vs. Schematic (LVS) to ensure it matches the logic.
Module 4: 4. Specialized Tracks & Advanced Topics Analog & Mixed-Signal Design: Designing op-amps, ADCs/DACs, and PLLs. FPGA Prototyping: Mapping designs onto Xilinx or Altera FPGAs for hardware testing. Low Power Design: Techniques like clock gating, power gating, and multi-voltage domains to save battery life. Design for Testability (DFT): Adding "scan chains" and BIST (Built-In Self-Test) to the chip

Programme Coordinator:

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Registration:
Registration is open to faculty, working professionals, industry persons, doctoral, postgraduate and graduate students from India and rest of the world. Participants will be

(A) Fee once paid will not be refunded back.
(B) The fee covers online participation in the programme, tutorial notes and examination, certification charges etc.
(C) The registration amount may be paid through online mode - NEFT / UPI / Cards / SWIFT, provided at the registration portal.
(D) Detailed schedule will be shared after receiving registration form.
→ For queries, **email us at fdp.academy@mnit.ac.in**

admitted on first-come first-served basis. Register online at(http://online.mnit

Mode of programme	Academia (faculty/Students): India/SAARC/Africa	Others: India/SAARC/Africa	Rest of the world
Online	Rs. 500/-	Rs. 1000/-	US $ 60/-

MNIT Jaipur one of the oldest NITs, the institute has a rich heritage of sixty years producing world class engineers, managers, architects and scientists. Ranked 43rd nationally in the NIRF ranking-2024 (Engineering), the institute offers learning opportunities for undergraduate, postgraduate students, and researchers in various domains. Having a lush green campus of over 317 acres within the heart of the pink city, close to Jaipur International Airport, the campus offers a safe and lively environment. A world class teaching infrastructure, state-of-art laboratories welcome you at the campus. The institute has a vision to impart education of international standards and conduct research atthe cutting edge of